

CLAIMS

Having thus described the invention, what is claimed is:

- 1        1. A method of fabricating at least a pair of local interconnects with  
2        one interconnect on each side of a gate of a field effect transistor (FET) in an  
3        integrated circuit on a semiconductor substrate comprising the steps of:  
4        forming on a semiconductor substrate a thick insulating layer;  
5                forming at least a pair of spaced apart openings in the insulating layer  
6        adjacent the semiconductor substrate;  
7                forming a source in one of the openings and a drain in the other of  
8        the openings;  
9                filling each of the openings with a conductive material to form local  
10      interconnects to the source and drain;  
11               removing a portion of the insulating layer to form a gate opening  
12      between the local interconnects;  
13               forming a gate dielectric on the semiconductor substrate in the gate  
14      opening; and  
15               forming a gate on the gate dielectric oxide in the gate opening  
16      between the local interconnects.
- 1        2. The method of Claim 1, wherein the space between the pair of  
2        openings is one minimum photolithographic feature and the local interconnects are  
3        each one minimum photolithographic feature.
- 1        3. The method of Claim 1, wherein insulating spacers are each  
2        disposed on an interconnect wall adjacent the gate to separate each of the local  
3        interconnects from the gate.

1                   4. The method of Claim 1, wherein the source and drain are formed  
2 by implanting impurities in the pair of openings in the insulating layer.

1                   5. The method of Claim 1, wherein the portion of insulating layer  
2 removed to form the gate opening is removed by using a masking material with an  
3 opening in the masking material positioned between the pair of local interconnects.

1                   6. The method of Claim 5, wherein the opening in the masking  
2 material extends over but not beyond each of the pair of local interconnects.

1                   7. The method of Claim 6, wherein the spaced apart openings are  
2 positioned over an active region in the semiconductor substrate, the active region  
3 being surrounded by an isolation region, the openings extending to or beyond the  
4 active region.

1                   8. The method of Claim 1, wherein a conductive layer is formed on  
2 the walls of the spaced apart openings to line the openings and a remainder of the  
3 local interconnect openings are filled with another conductive material.

1                   9. The method of Claim 8, wherein the conductive layer is  
2 polysilicon and the other conductive material is tungsten.

1                   10. The method of Claim 9, wherein the polysilicon is the origin for  
2 the impurities for the source and drain.

1                   11. The method of Claim 1, wherein a barrier layer is formed on  
2 walls of the local interconnect openings to line the opening and a remainder of the  
3 local interconnect opening is filled with a conductive material.

1                   12. The method of Claim 11, wherein the barrier layer includes  
2                   titanium nitride.

1                   13. The method of Claim 1, wherein an insulating etch stop layer is  
2                   formed on semiconductor substrate before forming the thick insulating layer.

1                   14. The method of Claim 13, wherein the etch selectivity of the etch  
2                   stop layer is different from the etch selectivity of the insulating layer.

1                   15. The method of Claim 14, wherein the etch stop layer is a nitride  
2                   of silicon.

1                   16. The method of Claim 1, wherein the gate is selected from the  
2                   group of polysilicon, refractory metal and metal.

1                   17. In a method of fabricating, in an integrated circuit on a  
2                   semiconductor substrate, a field effect transistor (FET) having a source, drain and  
3                   gate and with one interconnect on each side of a gate of the FET comprising the  
4                   steps of:

5                   forming on a semiconductor substrate a thick insulating layer;

6                   forming a pair of spaced apart openings in the insulating layer  
7                   adjacent the semiconductor substrate, each opening being the size of a minimum  
8                   lithographic feature;

9                   forming a source in one of the openings and a drain in the other of  
10                  the openings;

11                  filling each of the openings with a conductive material to form local  
12                  interconnects to the source and drain;

removing a portion of the insulating layer to form a gate opening of a minimum lithographic feature between the local interconnects; and

13. removing a portion of the insulating layer to form a gate opening of a  
14. minimum lithographic feature between the local interconnects; and

15. forming a gate in the gate opening between the local interconnects,  
16. whereby the size of the FET transistor is three minimum lithographic features.

1                   18. The method of Claim 17, wherein openings in the insulating  
2 material are positioned over an active region in the semiconductor substrate, the  
3 active region being surrounded by an isolation region, and the openings extending  
4 to or beyond the active region.

1                   19. An integrated circuit including at least one transistor, the  
2 integrated circuit comprising:

3                   a pair of local interconnects spaced from each other by a minimum  
4                   lithographic feature and each being a minimum lithographic feature; and  
5                   a gate of the transistor disposed in the space between the local  
6                   interconnects and separated from each of the local interconnects by an insulating  
7                   liner, whereby the width of the transistor is not greater than three lithographic  
8                   features.

1                    21. An integrated circuit including at least one transistor, the  
2 integrated circuit comprising:  
3                    a pair of local interconnects spaced from each other; and

4                   a gate of the transistor disposed in the space between the local  
5                   interconnects and separated from each of the local interconnects by an insulating  
6                   liner.

1                   22. The integrated circuit of Claim 21, wherein the pair of local  
2                   interconnects are spaced from each other by a minimum lithographic feature.

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